ADVANTAGES OF FLIP CHIP TECHNOLOGY IN MILLIMETER-WAVE PACKAGING

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Abstract **- Power leakage into surface waves in monolithically integrated millimeter-wave circuits is to a great extent determined by the applied packaging technology. In this presentation it is shown that properly designed flip chip packages will not suffer from surface wave leakage. Coplanar waveguides on GaAs substrates are used to demonstrate the decisive differences in the leakage behavior of flip chip mounted MMICs and more conventional MMW packages, featuring surface mounted MMICs connected by wire bonds. All results are based on full wave spectral domain analysis and measurement data in the frequency range from 10 to 120 GHz.**

I. INTRODUCTION

Emerging commercial applications in the range of millimeter-wave (MMW) frequencies have stimulated the need for suitable packaging technologies which are low-cost and still satisfy the sensitive demands incorporated in millimeter-wave subsystems [1]. The application of the coplanar waveguide technology has not only led to a reduction in MMIC manufacturing cost, it has also encouraged the use of flip chip as an alternative packaging technology for millimeter-wave subsystems [2, 3]. At the same time, it has been pointed out, that conventionally packaged MMW integrated circuits mounted on a metallized surface and connected by wire bonds will suffer from enhanced power leakage into surface waves [4] and high interconnection loss [5]. In this study, we show that unwanted packaging effects due to surface wave leakage can be avoided through the application of the flip chip technology. We use coplanar waveguide (CPW) transmission lines on GaAs substrates with dimensions commonly used in millimeter-wave designs to demonstrate the decisive differences in the performance of surface mounted and flip chip assembled coplanar MMICs. All results presented are based on full wave analysis and measurement data in the entire frequency range from 10 to 120 GHz.

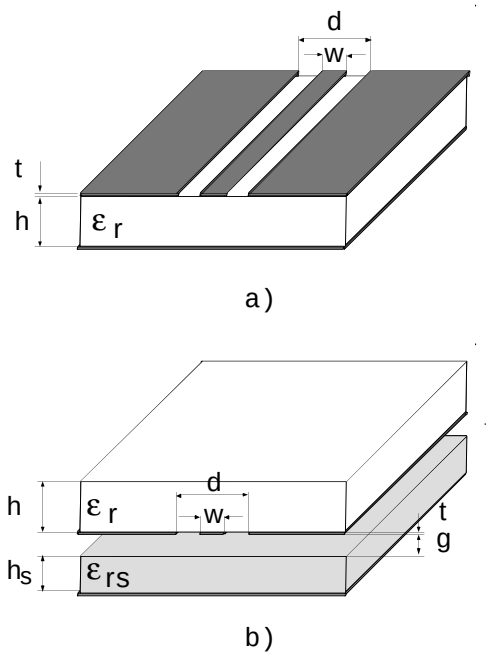

Fig. 1 Coplanar waveguides (CPW) in different mounting configurations: a) CPW with conductor backing (CBCPW) due to mounting on metallized package surface b) flip chip assembled CPW with uncovered backside facing the surface of the mounting substrate.

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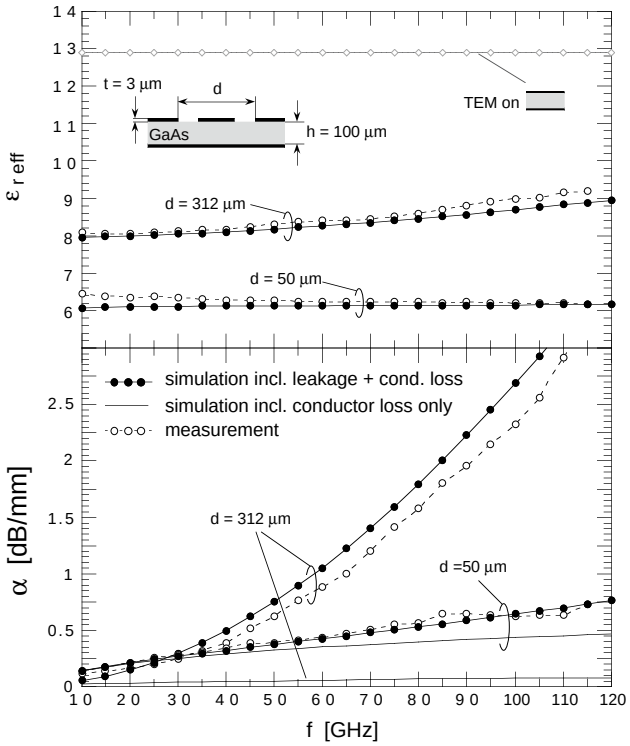

Fig. 2 Simulated and measured values for the propagation constants of CBCPWs on GaAs substrates (ε_r = 12.9, h = 100 µm). The chosen line dimensions are d = 312 µm (w = 120 µm) and d = 50 µm (w = 17 µm), the thickness of the Au metallization is t = 3 µm ($\rho = 3.0 \cdot 10^{-8}$ Ωm). Also shown are the attenuation constant due to conductor loss only and the propagation constant of the TEM surface wave of the background waveguide.

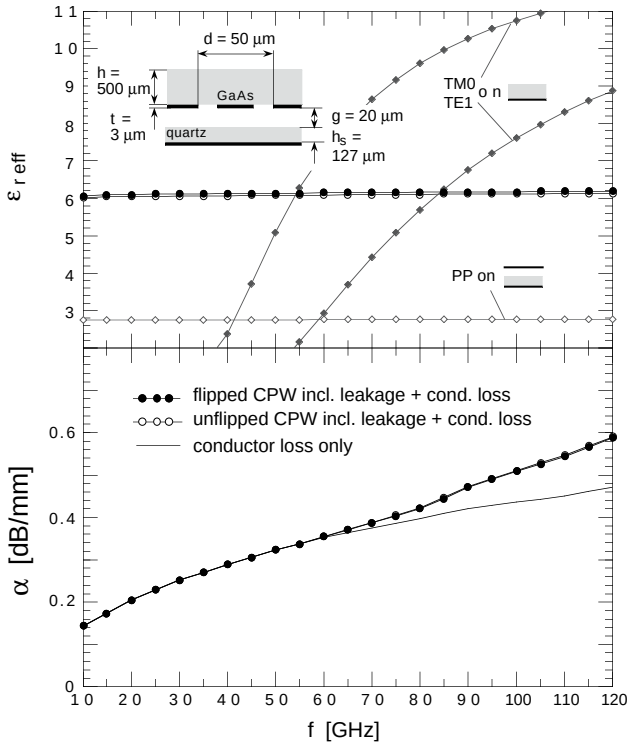

Fig. 3 Simulated values for propagation constants of a CPW on GaAs substrate (ε_r = 12.9, h = 500 µm, d = 50 µm, w = 17 µm, t = 3 µm) flip chip mounted on quartz substrate (ε_r = 3.8, h_s = 127 µm, g = 20 µm). Also shown are the values for $\varepsilon_{r\,eff}$ for the unflipped CPW (α curves are almost identical) and for the characteristic surface waves.

II. SURFACE MOUNTING

The packaging of millimeter-wave systems is in most cases done by first mounting the MMICs on a metallized package surface, and then wire bonds are used to make the interconnects. Thereby, a conductor backing for the planar circuits is introduced (Fig. 1a). The presence of this backside metallization makes coplanar transmission lines suffer from power leakage into the TEM surface wave at all frequencies. Since this leakage strongly depends on the line dimensions and the thickness of the substrate, we have studied the characteristics of conductor backed CPWs (CBCPWs) on GaAs with line dimensions that cover the range of values found in most millimeter wave applications. The obtained results are a useful indication for the increased power loss and unwanted cross talk to be expected after the circuits were assembled in the package. Fig. 2 shows simulated and measured values for the transmission line parameters $\varepsilon_{r\,eff}$ and α, including leakage and conductor loss, of surface mounted CPWs having ground-to-ground spacings of d = 50 µm and d = 312 µm. The GaAs substrate is thinned down to h = 100 µm as it is commonly done to improve heat sinking capability [6]. Evidently, the guided wave on the larger line experiences considerable attenuation due to leakage making it inappropriate for technical applications. The agreement between the simulated and measured data is reasonably good which confirms the validity of the analysis (the discrepancy is caused by the truncation of the substrate). The line with d = 50 µm shows an attenuation due to surface wave leakage which is much smaller, it is, however, still of the order of the conductor losses at high frequencies.

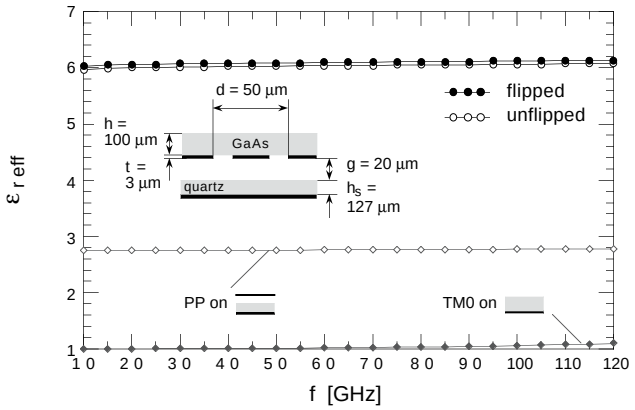

Fig. 4 Simulated values for the propagation constant of a CPW on GaAs substrate (ε_r = 12.9, h = 100 µm, d = 50 µm, w = 17 µm, t = 3 µm) flip chip mounted on a quartz carrier substrate (ε_r = 3.8, h_s = 127 µm, g = 20 µm). Also shown are the values for $\varepsilon_{r\,eff}$ for the unflipped CPW and for the characteristic surface waves. The α curves are not shown, since no leakage occurs.

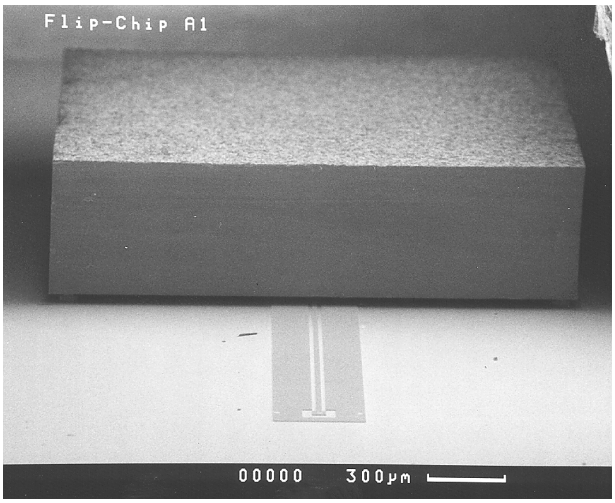

Fig. 5 Flip chip test structure consisting of flipped GaAs CPW (l = 4.7 mm) mounted on conductor backed GaAs carrier with coplanar feed lines (l = 2 mm). The bumping process and the flip chip mounting were performed by Alcatel SEL AG, Stuttgart, Germany.

III. FLIP CHIP MOUNTING

The use of flip chip leaves the backside of the assembled circuits uncovered. However, the chip surface now faces the grounded mounting substrate (Fig. 1b). On the one hand this leads to small changes in the propagation constant and characteristic impedance caused by the proximity to the dielectric or metallized surface of the carrier [5]. On the other hand additional surface waves are supported by the inhomogeneously filled parallel plate waveguide formed between the chip metallization and the conducting backside of the mounting substrate. The excitation of these surface waves depends on the choice of the carrier substrate and its thickness as well as on the size of the air gap between chip and carrier which is given by the height of the bumps. We show here the results for coplanar waveguides on GaAs substrates flip chip mounted on a quartz carrier substrate (h_s = 127 µm). Fig. 3 illustrates the simulated propagation constants for a CPW with d = 50 µm on GaAs (h = 500 µm). The height of the gap between chip and carrier is g = 20 µm. The upper part of the plot shows the $\varepsilon_{r\,eff}$ of the flipped and the unflipped CPW revealing only a minor change. The surface waves shown are the characteristic surface waves of the grounded dielectric slab and the surface wave of the inhomogeneously filled parallel plate wave-

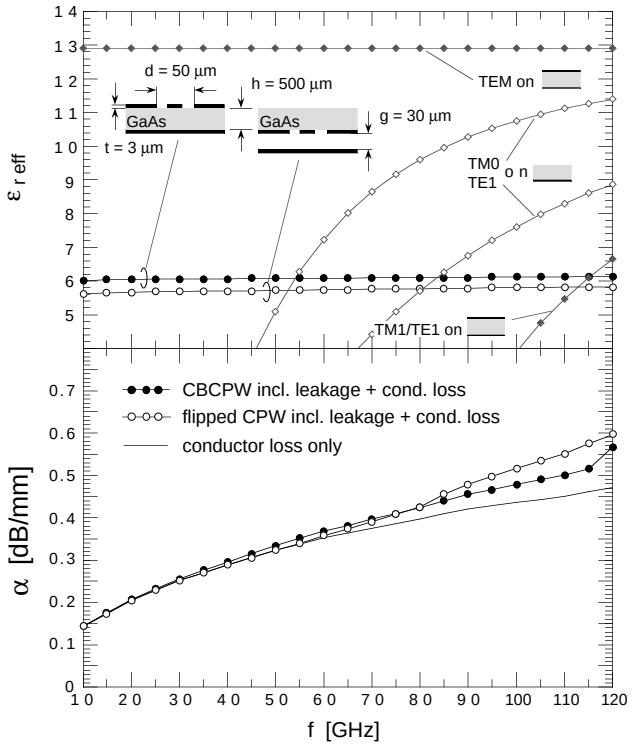

Fig. 6 Simulated values for propagation constants of the CPWs found in the test structure of Fig. 5. a) feed lines: CBCPW on GaAs (ε_r = 12.9, h = 500 µm, d = 50 µm, w = 17 µm, t = 3 µm). b) flipped CPW on GaAs: (ε_r = 12.9, h = 500 µm, d = 50 µm, w = 17 µm, t = 3 µm).

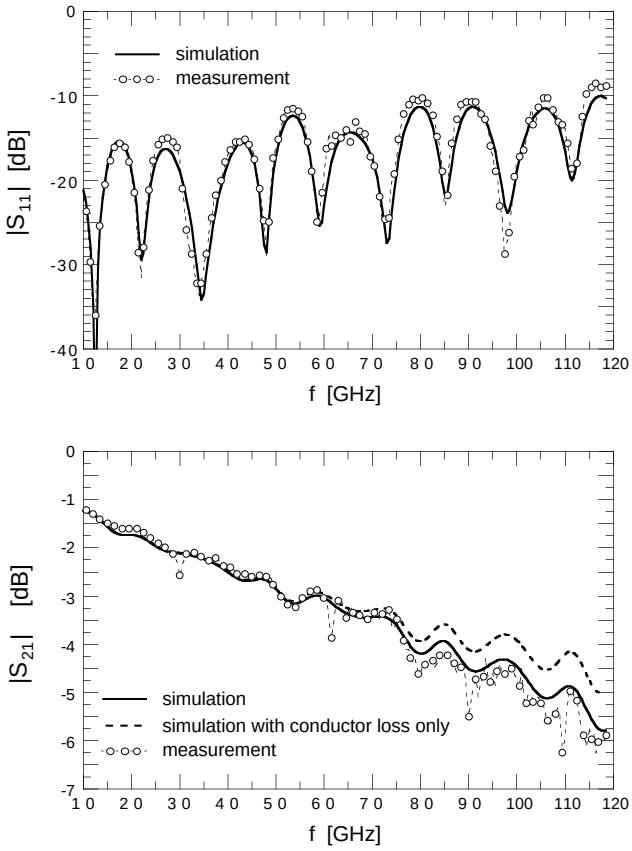

Fig. 7 Measured and simulated S-parameters of the flip chip test structure consisting of a CPW on GaAs mounted on a GaAs carrier substrate (Figs. 5 and 6).

guide below the CPW. Obviously, the parallel plate mode is always faster than the propagating wave on the CPW and therefore no leakage into this surface wave occurs. Thus, the additional attenuation depicted in the lower part of the plot is only due to the grounded dielectric slab formed by the chip itself. Consequently, in this case thinning of the GaAs chip is advantageous and leads to a complete avoidance of surface wave leakage in the frequency range of interest. Fig. 4 illustrates this case for a GaAs chip with h = 100 μm. The attenuation constant is not shown since it is equal to the conductor loss only.

Experimental investigation of surface wave leakage in flip chip packages has been carried out using several different test structures consisting of CPWs on GaAs (length = 4.7 mm) that were flip chip mounted on a GaAs carrier substrate with conductor backed coplanar feed lines (length = 2 mm). One of the test pieces is shown in Fig. 5. The corresponding propagation constants for the feed lines and the mounted line are given in Fig. 6 (also in [5]). Note that the carrier surface is metallized underneath the chip in this case. The interconnection itself is modeled by an appropriate transmission line model [5]. Fig. 7 shows that the measured and simulated S-parameters of the entire test structure are in good agreement. For comparison the transmission coefficient $|S_{21}|$ excluding leakage is also shown which illustrates the significance of the leakage effect at high frequencies.

V. REFERENCES

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